Claims

(1) A liquid crystal display device having a liquid crystal display matrix comprised of individual pixels at the intersections of scan lines and data lines, a scan line driving circuit to drive said scan lines, and a data line driving circuit to drive said data lines, and, in said data line driving circuit, a single shift register having at least as many stages as the number of said data lines;

and characterized by, in said single shift register, the simultaneous shifting of multiple mutually spaced pulses; and, from this, the parallel output of multiple mutually spaced pulses from the output terminals of each stage of said shift register for the purpose of determining the operation timing of the circuits comprising said data line driving circuit.

(2) In Claim 1, a liquid crystal display device characterized by said data line driving circuit having multiple switch circuits corresponding to each data line for sampling of video signals;

and each of said multiple pulses being used to determine the sampling timing of the video images from each of the multiple switch circuits.

(3) In Claim 2, a liquid crystal display device characterized by multiplexing of said video signal in

proportion to the number of multiple, mutually spaced, parallel pulses.

(4) In Claim 3, a liquid crystal display device characterized by having a total number of said multiple, mutually spaced, parallel pulses of N (N is a natural number of two or greater);
and, having said multiple switch circuits divided into a total of N groups in which each group is comprised of M (M is a natural number of two or greater) switch circuits;
and, having N video signal input lines for the purpose of inputting the said video signal in which a single group of said M switch circuits is connected in common to a single video signal line.

(5) In Claim 1, a liquid crystal display device characterized by said data line driving circuit having a latch circuit which temporarily stores the digitized video signal and this latch circuit having at least as many bits as the number of said data lines;
and said multiple pulses each being used to determine the latch timing of the video signal contained in each bit of said latch circuit.

(6) In Claim 5, a liquid crystal display device characterized by multiplexing of said video signal in

proportion to the number of multiple, mutually spaced, parallel pulses.

(7) In Claim 6, a liquid crystal display device characterized by having a total number of said multiple, mutually spaced, parallel pulses of N (N is a natural number of two or greater);
and, having N M-bit (M is a natural number of two or greater) latch circuits;
and, having N video signal input lines for the purpose of inputting the said video signal in which each of said N latches is connected to one of N video signal input lines.

(8) In Claim 1, a liquid crystal display device characterized by having multiple gate circuits into which each output of multiple adjacent stages of said shift register is input, and in which each output of these gate circuits is used as the timing control signal of the circuits comprising the data line driving circuit.

(9) In Claim 8, a liquid crystal display device characterized by said multiple gate circuits being an EXCLUSIVE-OR circuit.

(10) In Claim 1, a liquid crystal display device characterized by having the number of gate circuits correspond to the number of stages of said shift register

and having the output of each stage of said shift register as an input to the gate circuits, and having each output of these gate circuits used as the timing control signal of the circuits composing the data line driving circuit;
and, further, by inputting an output enable signal to each said gate circuit to stop level changes in the output signal of the gate circuits.

(11) In Claim 10, a liquid crystal display device characterized by fixing the said output enable signal at a prescribed level during the blanking period in which a video signal is not input, and thereby forcing the stoppage of level changes in the output signal of each said gate circuit.

(12) In Claim 1, an active matrix liquid crystal display device which drives each liquid crystal display pixel by means of a switching element;
and a liquid crystal display device which is characterized by at least a portion of the transistors which comprise said data line driving circuit being formed on the active matrix substrate using the same fabrication process as said switching elements.

(13) In Claim 12, a liquid crystal display device characterized by the fact that the transistors comprising

said switching elements and said data line driving circuit are thin film transistors (TFTs).

(14) A liquid crystal display device characterized by having individual liquid crystal display pixels at the intersections of scan lines and data lines and switching elements connected to these liquid crystal display pixels;
and a scan line driving circuit which drives said scan lines;
and a data line driving circuit which drives said data lines;
and an inspection signal circuit which can collectively input a signal for inspection using a first terminal of each of said data lines;
and further characterized by the fact that said data line driving circuit has a single shift register having at least as many stages as the number of said data lines and multiple switch circuits which have the function of supplying a liquid crystal display signal by means of a second terminal located on the opposite end of each said data line as that of said first terminal;
and each switch circuit being connected to input lines for inputting said liquid crystal display signal;
and further characterized by the fact that within said single shift register, a single pulse is sequentially shifted resulting in a single pulse being sequentially output from the output terminal of each stage of said

shift register and these pulses being used to sequentially turn on said multiple switch circuits.

(15) In Claim 14, a liquid crystal display device characterized by at least a portion of the transistors which comprise said data line driving circuit being formed on the active matrix substrate using the same fabrication process as the switching elements comprising said active matrix.

(16) In Claim 15, a liquid crystal display device characterized by the fact that the transistors comprising said switching elements and said data line driving circuit are thin film transistors (TFTs).

(17) A liquid crystal display device driving method for a liquid crystal display device having individual pixels at the intersections of the scan lines and data lines characterized by the establishment, as an essential component of the driving circuit for said data lines, of a single shift register having at least as many stages as the number of said data lines,
and further characterized by realizing a state in which a single same-polarity pulse is input in the input terminal of the shift register after each horizontal period of the video signal, and, after waiting for at least (N-1) horizontal periods, N mutually spaced, parallel pulses

are output from the output terminals of each stage of said shift register;
and said data lines are driven using said N pulses as the timing control signal for the circuits comprising said data line driving circuit.

(18) In Claim 17, a liquid crystal display device driving method characterized by the fact that said video signal is made into parallel components in proportion to the number of said multiple, mutually spaced, parallel pulses (N),
and further characterized by the fact that the clock frequency driving said shift register is 1/N or less of the frequency of the original video signal prior to being made into parallel components.

(19) A liquid crystal display device driving method for a liquid crystal display device having individual pixels at the intersections of the scan lines and data lines characterized by the establishment, as an essential component of the driving circuit for said data lines, of a single shift register having at least as many stages as the number of said data lines and multiple EXCLUSIVE-OR circuits having as inputs the adjacent outputs of the multiple stages of this shift register;
and further characterized by realizing a state in which a pulse is input in the input terminal of said shift register after one cycle corresponding to two horizontal

periods of the video signal, and multiple, mutually spaced, parallel pulses are output from the output terminals of each stage of said shift register; and said data lines are driven using said multiple pulses as the timing control signal for the circuits comprising said data line driving circuit.

(20) A liquid crystal display device inspection method characterized by having an active matrix in which individual liquid crystal display pixels are formed at the intersections of scan lines and data lines and switching elements are connected to these liquid crystal display pixels; and a scan line driving circuit which drives said scan lines; and a data line driving circuit which drives said data lines; and an inspection signal circuit which can collectively input a signal for inspection using a first terminal of each of said data lines; and further characterized by the fact that said data line driving circuit has a single shift register having at least as many stages as the number of said data lines and multiple switch circuits which have the function of supplying a liquid crystal display signal by means of a second terminal located on the opposite end of each said data line as that of said first terminal; and each switch circuit being connected to input lines for inputting said liquid crystal display signal;

and, by means of input circuits for said inspection signal, said inspection signal is input at the first terminal on each said data line;

and while maintaining such an input state, a single pulse is sequentially shifted within said single shift register, and, accordingly, single pulses are sequentially output from the output terminals of each stage of said shift register, and these pulses are used to sequentially turn on said multiple switch circuits, and, as a result, said switch circuits turn on sequentially and consequently said inspection signal sent from one terminal of said data lines is received through said switch circuits and said input lines for inputting said liquid crystal display signal and inspection of the electrical characteristics of said data lines and said switch circuits is performed.

(21) In Claim 20, a liquid crystal display device inspection method characterized by the fact that when a specific data line and the switch circuit corresponding to said data line are inspected, the clock supply to said shift register is stopped; and, accordingly, only said specific switch circuit is on and inspection of said specific data line and corresponding switch circuit is performed.

Summary

Using technology which uses a single shift register and simultaneously generates multiple pulses, this invention is a liquid crystal display device which rapidly drives data lines.

It is possible to increase the frequency of the shift register output signal without changing the frequency of the shift register operation clock. If the shift register output signals, by means of analog switches, are used to determine the video signal sampling timing, high speed data line driving can be realized.

Additionally, if the output signals of the shift register mentioned above are used to determine the video signal latch timing in a digital driver, high speed latching of the video signal can be realized. Consequently, even if the driving circuits of the liquid crystal display matrix are composed of TFTs, high speed operation of the driving circuits is possible without increasing power consumption.

The shift register can also be used to inspect the electrical characteristics of the data lines and analog switches.